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In the Claims:

Please amend claims 1, 10 and 19 as follows.

1. (Currently Amended) In a microprocessor having a plurality of physical registers, a method for managing said plurality of physical registers, said method comprising steps of:

providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor, said destination operand identifying where data resulting from an operation is to be stored;

storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for an architectural register of a selected instruction executing on the microprocessor;

transferring said physical register assignment of said selected physical register from said second structure to a third structure after retirement of said selected instruction, the third structure holding information regarding a plurality of physical register assignments;

assigning said architectural register as a destination operand for a subsequent instruction; and

prior to the retirement of said subsequent instruction, transferring information identifying said selected physical register as soon-to-be available from said third structure to said first structure.

2. (Original) The method as recited in claim 1 further comprising the step of storing mappings of logical registers to said plurality of physical registers.

3. (Original) The method as recited in claim 2 wherein the microprocessor is comprised of a memory array and wherein said method further comprises the step of storing said mappings to the memory array.

4. (Original) The method as recited in claim 1 wherein said microprocessor simultaneously executes multiple threads.

5. (Previously Presented) The method as recited in claim 1 wherein contents of said first structure, second structure, and third structure are self-initialized to store mappings of said physical registers.

6. (Original) The method as recited in claim 1 wherein contents of said assigned available physical registers are flushed from said assigned available physical registers.

7. (Original) The method as recited in claim 1 further comprising the step of detecting whether said assigned available physical registers are being utilized by said microprocessor for execution.

8. (Original) The method as recited in claim 1 wherein said method is performed by hardware.

9. (Original) The method as recited in claim 1 wherein said method is performed by software.

10. (Currently Amended) In a microprocessor having a plurality of physical registers, a method for managing said plurality of physical registers, said method comprising steps of:

providing a first structure for holding information identifying available physical registers that are free to be assigned to a plurality of destination operands for instructions executing on the microprocessor, said plurality of destination operands identifying where data resulting from an operation is to be stored;

storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned to one of said plurality of destination operands for an architectural register of a selected instruction executing on the microprocessor;

providing a third structure for holding information regarding physical registers utilized during execution of instructions;

transferring said physical register assignment of said selected physical register from said second structure to a third structure after retirement of said selected instruction;

assigning said architectural register as a destination operand for a subsequent instruction; and

prior to the retirement of said subsequent instruction, transferring information identifying said selected physical register as soon-to-be available from said third structure to said first structure.

11. (Original) The method as recited in claim 10 further comprising the step of storing a plurality of mappings of logical registers to said plurality of physical registers.

12. (Original) The method as recited in claim 11 wherein the microprocessor is comprised of a memory array and wherein said method further comprises the step of storing said mappings to the memory array.

13. (Original) The method as recited in claim 10 wherein said microprocessor simultaneously executes multiple threads.

14. (Previously Presented) The method as recited in claim 10 wherein contents of said first structure, second structure, and third structure are self-initialized to store mappings of said physical registers.

15. (Original) The method as recited in claim 10 wherein contents of said assigned available physical registers are flushed from said assigned available physical registers.

16. (Original) The method as recited in claim 10 further comprising the step of detecting whether said assigned available physical registers are being utilized by said microprocessor for execution.

17. (Original) The method as recited in claim 10 wherein said method is performed by hardware.

18. (Original) The method as recited in claim 10 wherein said method is performed in software.

19. (Currently Amended) A microprocessor system with a plurality of physical registers for managing a plurality of physical register assignments comprising:

a first module for providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor, said destination operand identifying where data resulting from an operation is to be stored;

a second module for storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for an architectural register of a selected instruction executing on the microprocessor;

a third module for providing a third structure for holding information regarding physical registers utilized during execution of instructions;

a first interface for transferring said physical register assignment of said selected physical register from said second structure to said third structure after retirement of said selected instruction; and

a second interface for transferring information identifying said selected physical register as soon-to-be available from said third structure to said first structure subsequent to assignment of said architectural register as a destination operand for a subsequent instruction and prior to the retirement of said subsequent instruction.

20. (Original) The microprocessor as recited in claim 19 wherein said microprocessor simultaneously executes multiple threads.

21. (Canceled).